OCR
RECOGNISING ACHIEVEMENT

SPECIMEN

Advanced Subsidiary GCE

Electronics

Unit F612: Signal Processors

Specimen Paper

F612 QP

Candidates answer on the question paper.

Additional Materials:
Scientific calculator

Time:1 hour 30 mins

Candidate Name	

Centre Number						Candidate Number				

INSTRUCTIONS TO CANDIDATES

- Write your name, Centre number and Candidate number in the boxes above.
- Answer **all** the questions.
- Use blue or black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure you know what you have to do before starting your answer.
- Do **not** write in the bar code.
- Do **not** write outside the box bordering each page.
- WRITE YOUR ANSWER TO EACH QUESTION IN THE SPACE PROVIDED.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets [ ] at the end of each question or part question.
- You will be awarded marks for the quality of written communication where this is indicated in the question.
- You may use a scientific calculator.
- Unless otherwise indicated, you can assume that :
  - op-amps are run off supply rails at +15 V and -15 V
  - logic circuits are run off supply rails at +5 V and 0 V
- You are advised to show all the steps in any calculations.
- The total number of marks for this paper is **90**.

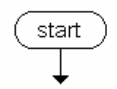
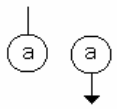
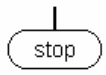
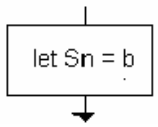
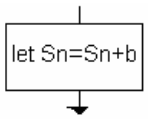
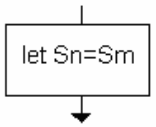
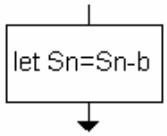
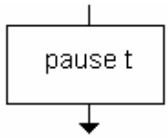
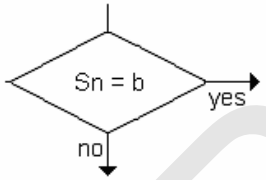
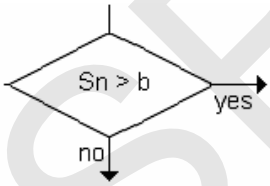
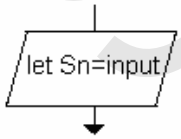
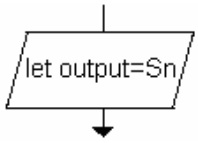
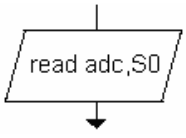
FOR EXAMINERS' USE		
Qu.	**Max.**	**Mark**
1	**5**	
2	**7**	
3	**9**	
4	**23**	
5	**12**	
6	**18**	
7	**16**	
TOTAL	**90**	

Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15 V and -15V
- logic circuits are run off supply rails at +5 V and 0 V

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$ $A + \overline{A} = 1$ $A.(B + C) = A.B + A.C$ $\overline{A.B} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}.\overline{B}$ $A + A.B = A$ $A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$

symbol	meaning
	start the program
	link to part of the program with the same label a
	stop the program
	place the byte b in register Sn
	add the byte b to the byte in register Sn
	copy the byte in register Sm into register Sn
	subtract the byte b from the byte in register Sn
	introduce a time delay of t milliseconds
	branch if the byte in register Sn is equal to the byte b
	branch if the byte in register Sn is greater than the byte b
	copy the byte at the input port to register Sn
	copy the byte in register Sn to the output port
	activate the analogue-to-digital converter and store the result in register S0

[Turn over

1 Fig. 1.1 shows an op-amp connected as a non-inverting amplifier.

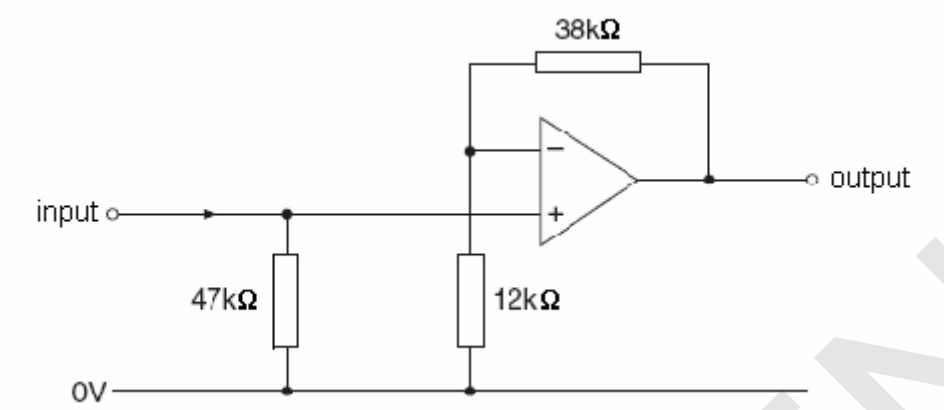


Fig. 1.1

(a) Show that the gain of the amplifier is about +4. **[2]**

(b) Fig. 1.2 is a voltage-time graph for a test signal at the input of the amplifier of Fig.1.1.

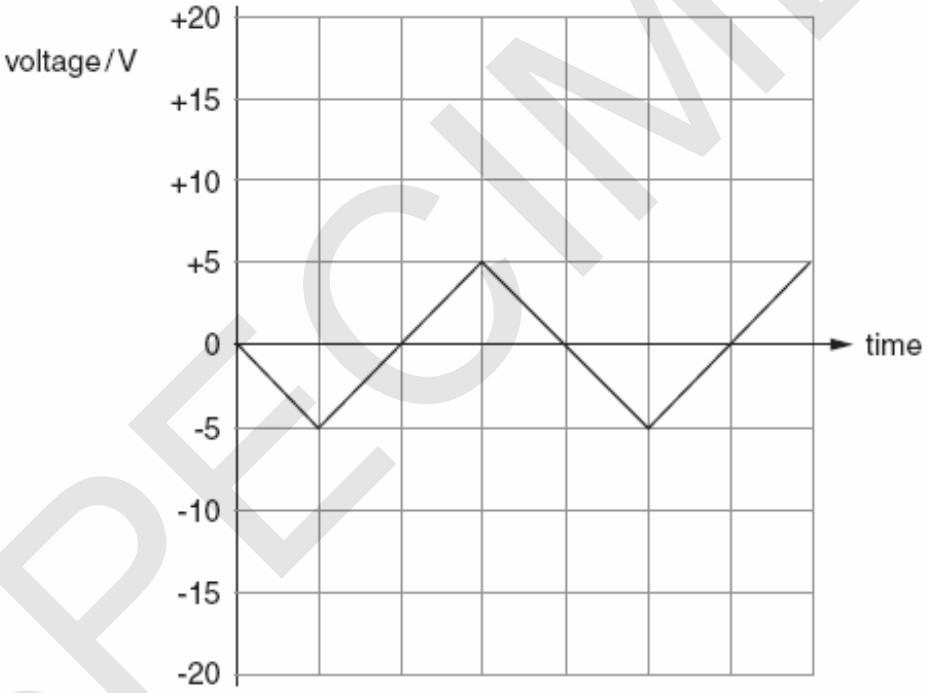


Fig. 1.2

Draw on Fig. 1.2 to show the signal at the output of the amplifier. **[3]**

2 The circuit of Fig. 2.1 uses a pair of D-type flip-flops Y, Z to indicate which input A or B receives a pulse first.

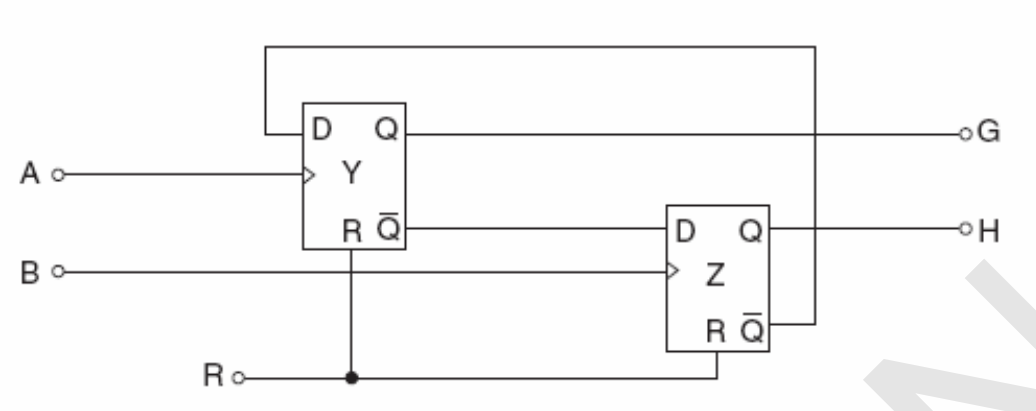


Fig. 2.1

(a) R is normally held low. State what happens to Q when R is pulsed high.

..... **[1]**

(b) Suppose that H is low when a pulse arrives at A.

Explain why this makes G go high.

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..... **[2]**

(c) Complete the timing diagram of Fig. 2.2.

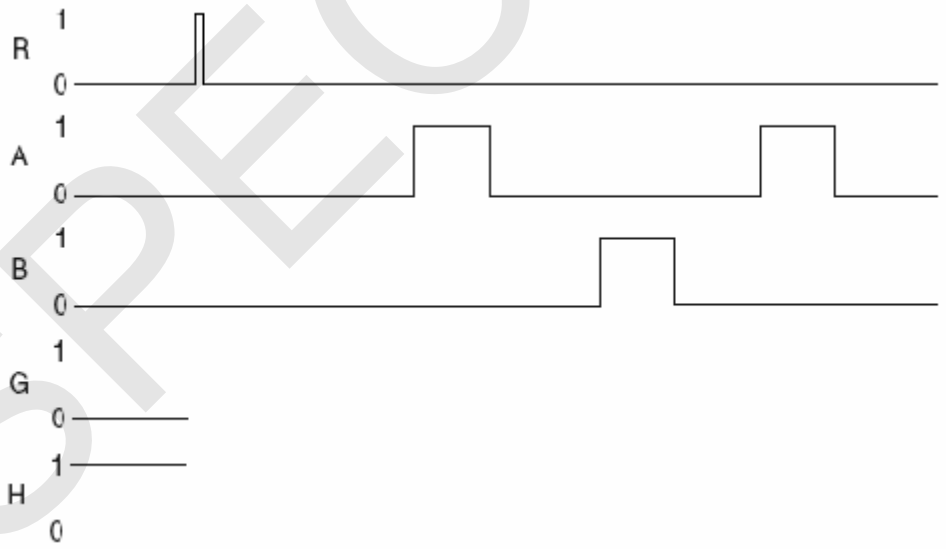

Fig. 2.2

[4]

3 **(a)** Draw on Fig. 3.1 the circuit diagram for an inverting amplifier with a voltage gain of –5.

The op-amp has been drawn already.

Show all component values and justify them.

Label the input and output of the inverting amplifier.

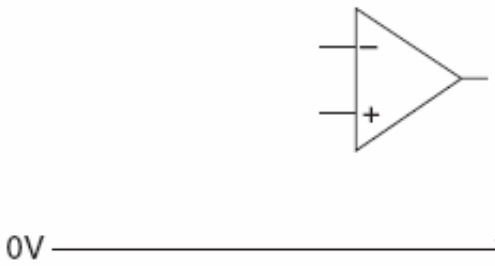

Fig. 3.1

[5]

(b) Draw on the axes of Fig. 3.2 to show how the output voltage of the inverting amplifier depends on its input voltage.

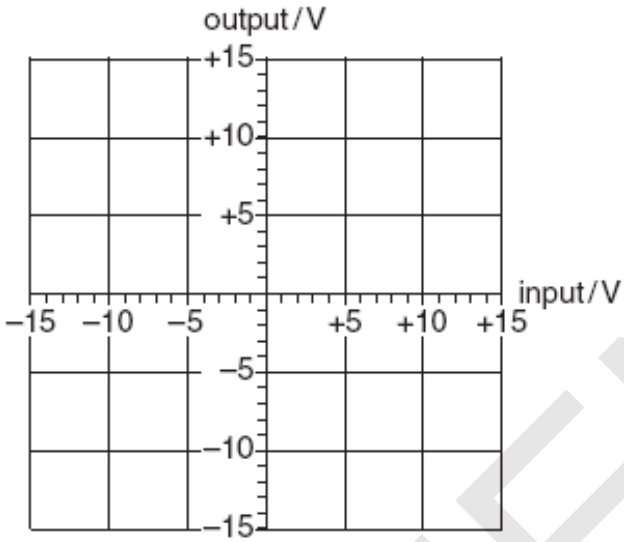

Fig. 3.2

[4]

4 Fig. 4.1 shows the diagram of a circuit containing a clock of frequency 1 Hz.

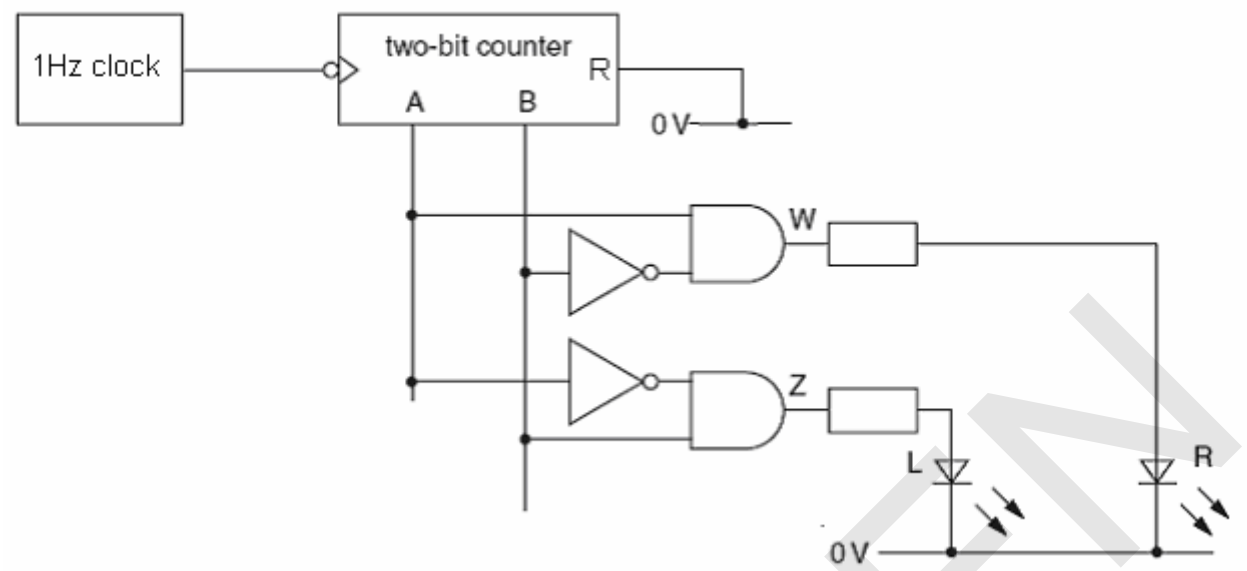

Fig. 4.1

(a) Complete Fig. 4.2 to show how a two-bit up-counter may be assembled from D-type flip flops and a NOT gate. Label the outputs A and B.

Fig. 4.2

[4]

(b) Complete the table below to show how the states of A and B together with the outputs W and Z and the on/off states of L and R will change with time.

clock pulse	A	B	W	Z	L	R
0	0	0			off	off
1						
2						
3						

[4]

(c) The circuit of Fig. 4.1 repeats a sequence of four states. Adapt the circuit so that it repeats the following sequence of three states.

clock pulse	L	R
0	on	off
1	on	on
2	off	on

(i) Complete Fig. 4.3 to show your adapted circuit.

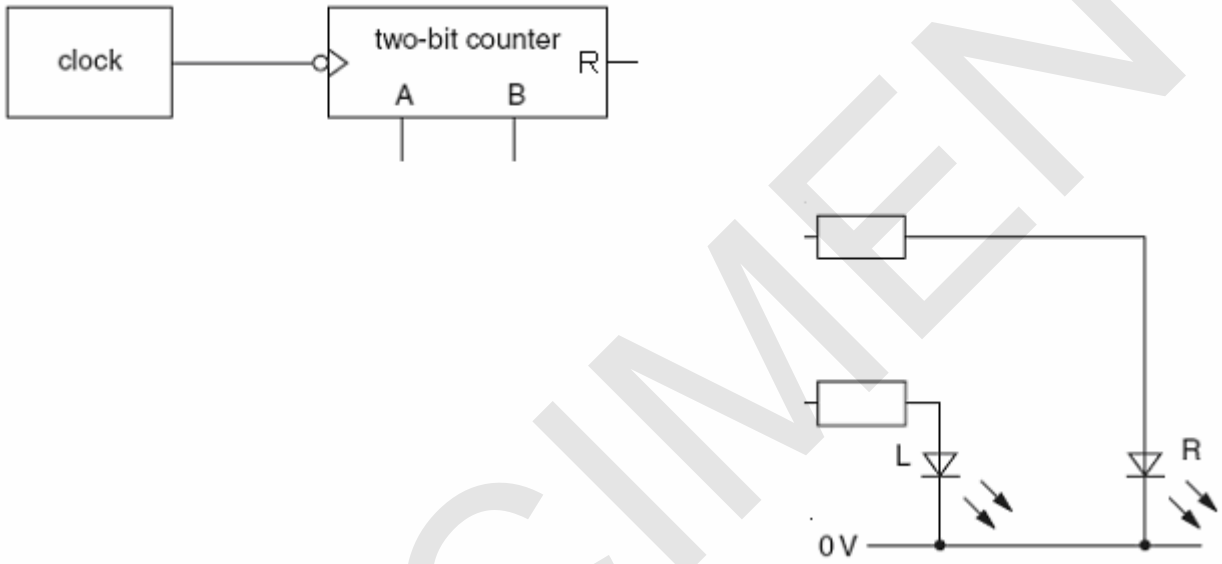

Fig. 4.3

[5]

(ii) Explain how your adapted circuit operates.

The quality of your written communication will be assessed in this question.

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..... **[7]**

(d) Circuits which generate sequences of signals can be made from microcontrollers.

Give **three** advantages of using a microcontroller instead of counters and logic gates for this type of circuit.

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..... **[3]**

[Turn over

5 **(a)** Using the op-amp in Fig. 5.1, complete the circuit for a **treble cut filter** with the following characteristics:

- maximum input resistance 33 kΩ
- low frequency gain –100
- break frequency 1000 Hz

Give component values and show your working for all calculations.

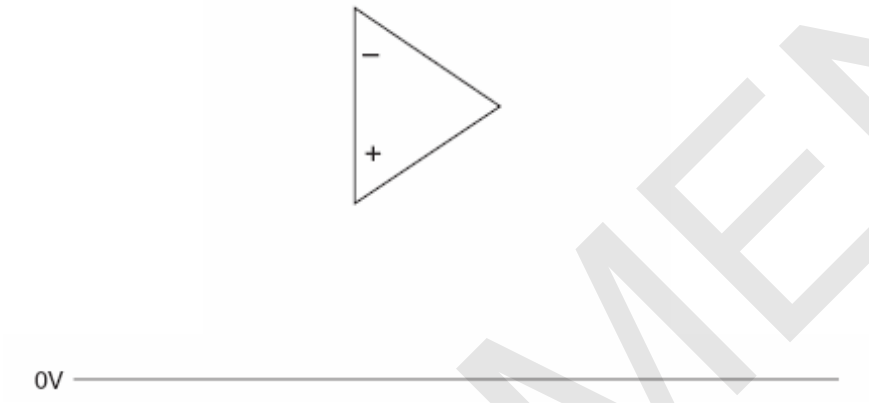

Fig. 5.1

[6]

(b) (i) On the axes of Fig. 5.2, draw the frequency response of your treble cut filter.

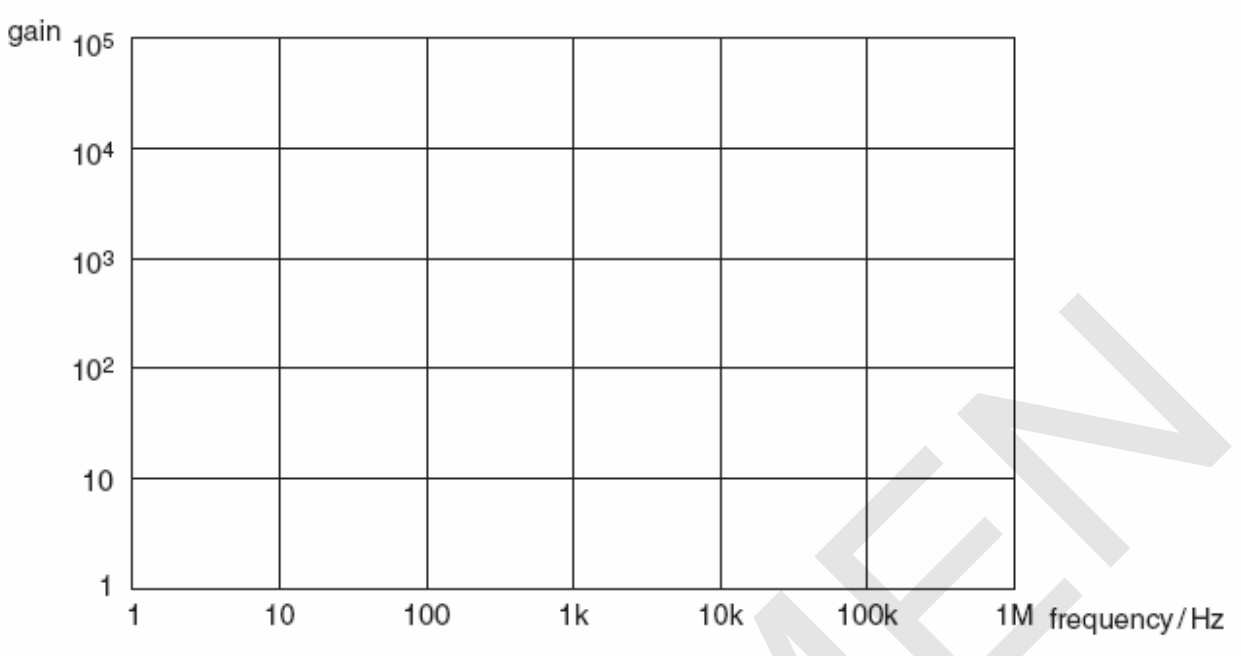

Fig. 5.2

[3]

(ii) Explain, in detail, why your circuit of Fig. 5.1 has the filtering action shown in the graph of Fig. 5.2.

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..... **[3]**

6 Fig. 6.1 shows a microcontroller providing an interface between two switches and a seven-segment LED.

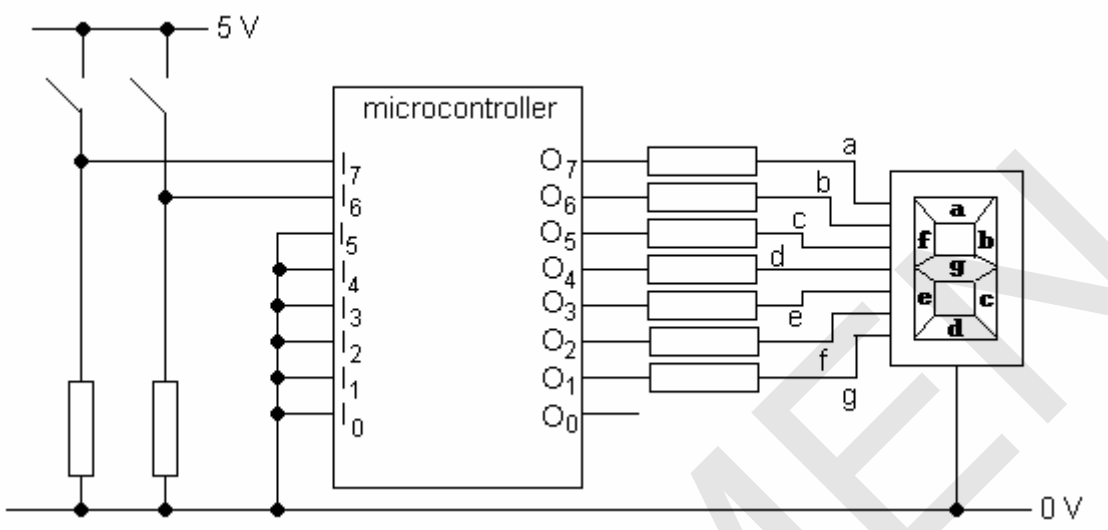

Fig. 6.1

(a) (i) What is a microcontroller?

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..... **[3]**

(ii) The behaviour of a microcontroller depends on hardware and software.

What is the difference between hardware and software?

.....

.....

.....

..... **[2]**

(b) Fig. 6.2 shows part of the program stored in the microcontroller's memory.

(i) The first instruction places the byte FD in register S2.

Write down the byte FD in binary.

..... **[1]**

(ii) Use the flowchart symbols on the Data Sheet to explain the function of each step of the program, **relating it to the circuit of Fig. 6.1**.

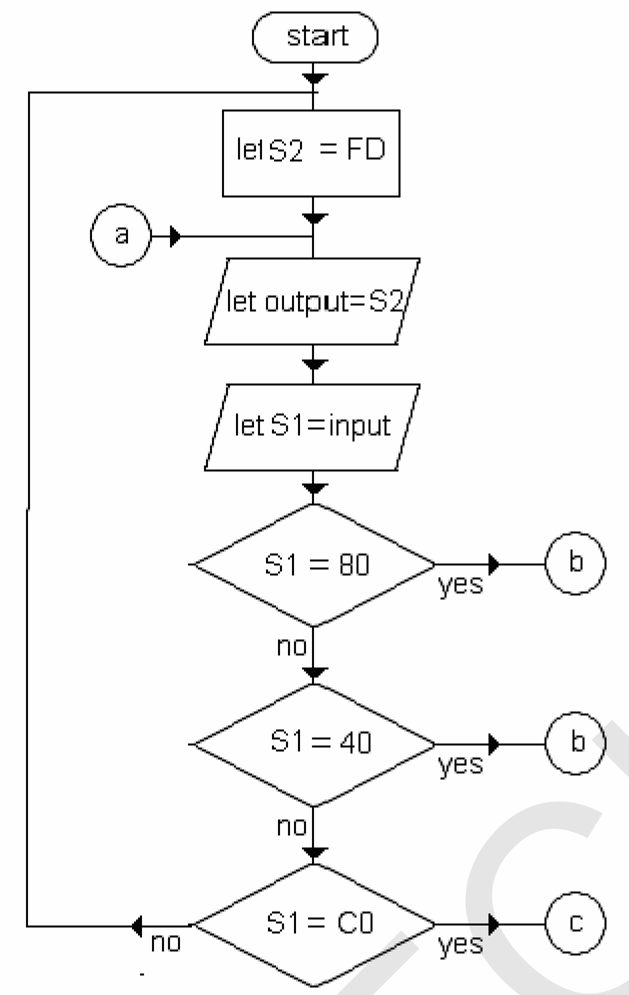

Fig. 6.2

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....[7]

(iii) The whole program makes the seven LEDs display the number of switches being pressed. In the space below, complete the program, using the flowchart symbols in the Data Sheet. Explain the function of each step.

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....[5]

[Turn over

7 Fig. 7.1 is an incomplete circuit of a mixer for a recording studio.

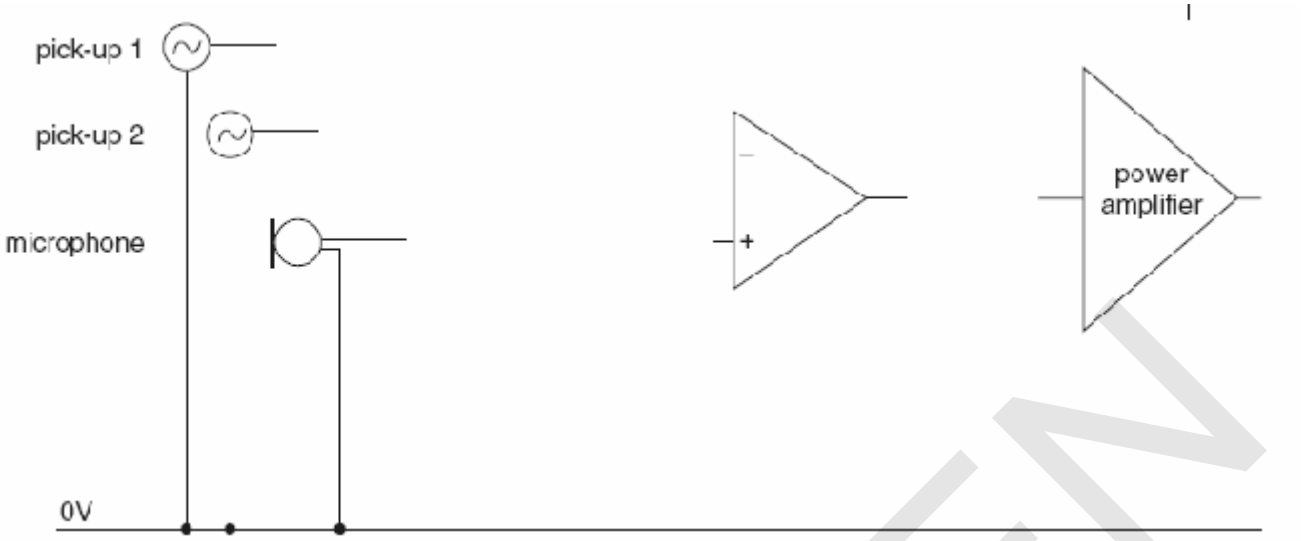

Fig. 7.1

The signals from the two guitar pick-ups and the microphone are mixed and amplified.

(a) (i) On Fig. 7.1, draw the circuit of a summing amplifier which will add the three inputs together.

No component values are needed at this stage. **[3]**

(ii) The student places a potentiometer as a volume control in the circuit.

On Fig. 7.1, show how the potentiometer should be connected. **[2]**

(b) Here are the peak output voltage of each of the three input signals.

Pick-up 1: ±20mV

Pick-up 2: ±20mV

Microphone: ±100 mV

(i) When only the microphone is used then the peak summing amplifier output should be ±5 V. The microphone should operate with an input resistor of 10 kΩ. Calculate a suitable value for the feedback resistor of the summing amplifier.

feedback resistance = ...kΩ **[3]**

(ii) When only one pick-up is used the peak summing amplifier output should be ±3 V.

Calculate suitable values for the remaining resistors of the summing amplifier.

pick-up input resistance = ...kΩ **[2]**

(c) A circuit for the power amplifier of Fig. 7.1 is shown in Fig. 7.2.

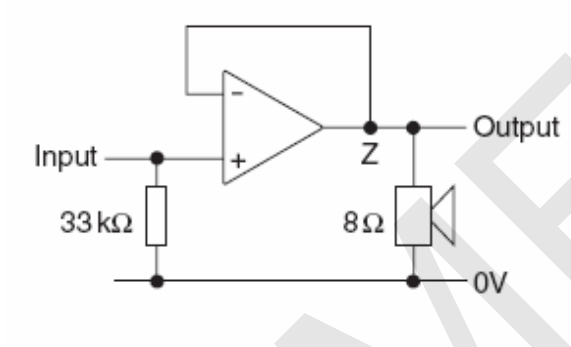

Fig. 9.2

The op-amp has negligible output impedance.

(i) Show that the op-amp must be able to supply a current of about 1.5 A at its output. Use information from (b)(i) and (b)(ii).

[3]

(ii) Explain why the circuit of Fig. 7.2 has a voltage gain of +1.

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..... **[3]**

Paper Total [90]

OCR RECOGNISING ACHIEVEMENT

OXFORD CAMBRIDGE AND RSA EXAMINATIONS

Advanced Subsidiary GCE

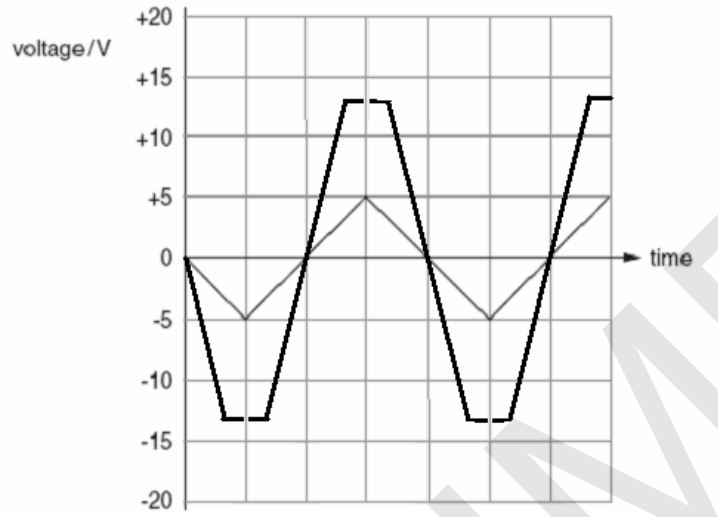
ELECTRONICS F612 MS

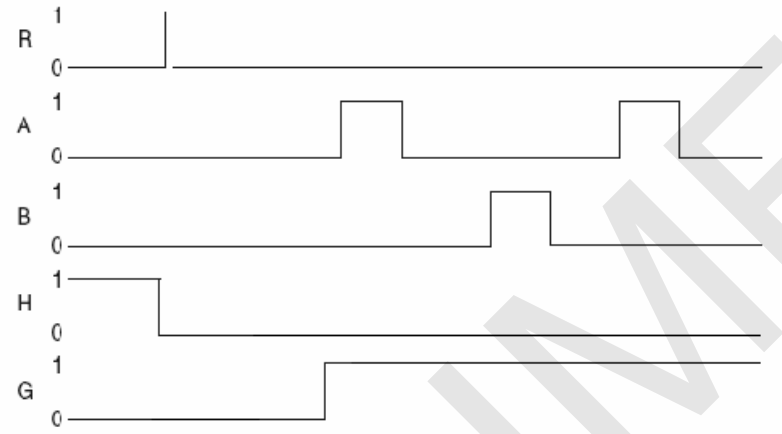
Unit F612: *Signal Processors*

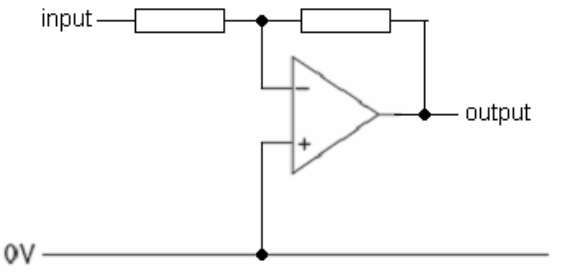
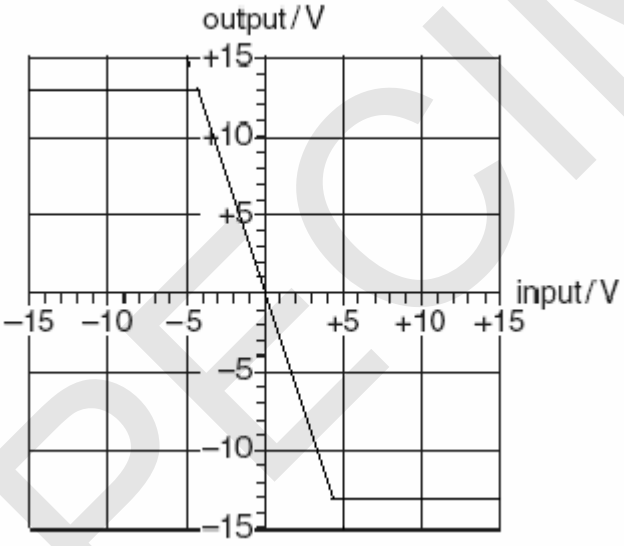
Specimen Mark Scheme

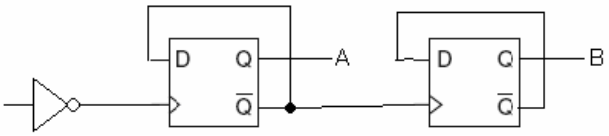
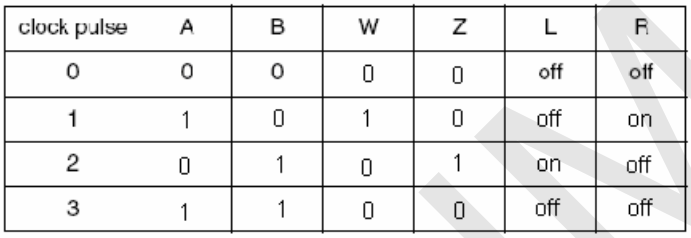
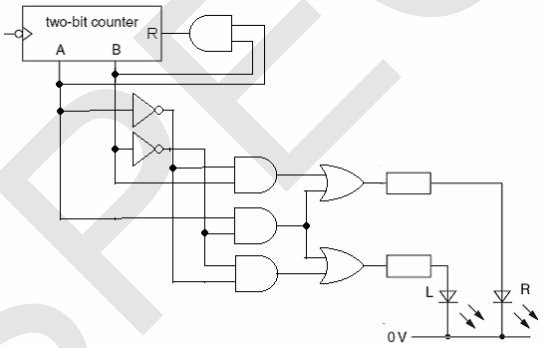
The maximum mark for this paper is **90**.

This document consists of **10** printed pages.

Question Number	Answer	Max Mark
1(a)	substitution: $G = 1 + (38/12)$ evaluation: $G = 4.1$	[2]
(b)	correct shape and phase (apart from saturation) correct gain (4) by eye saturation at ± 13 V (by eye)  	[3]

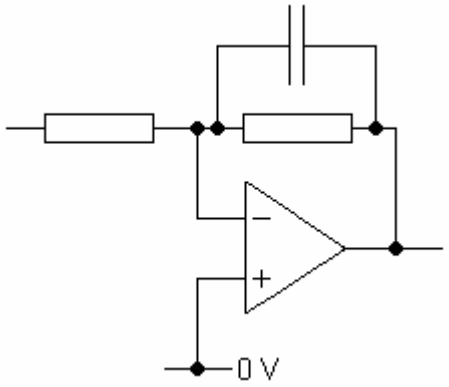
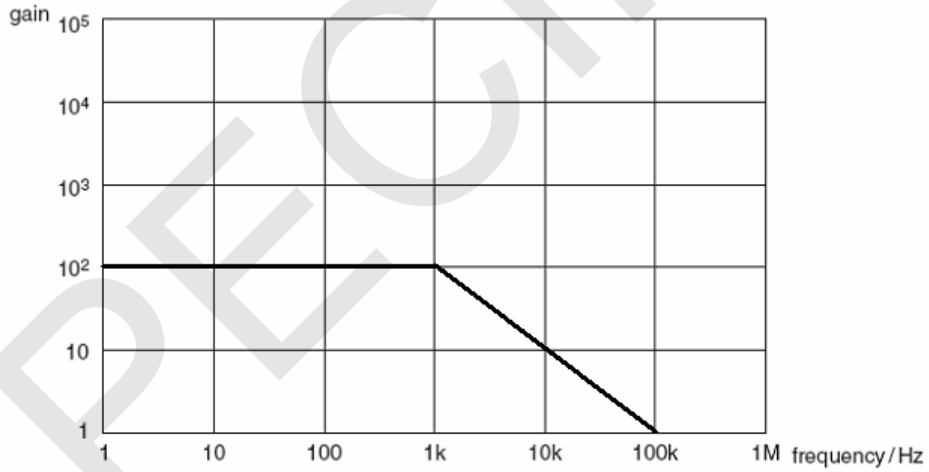
Question Number	Answer	Max Mark
2(a)	Q goes low / is reset	[1]
(b)	idea of $\overline{Q}$ being opposite state of Q idea of state of D transferred to Q	[2]
(c)	H goes low when R rises, G stays low subsequent changes of H and G only on rising edges of A or B G goes high and stays high on first rising edge of A H stays low after R goes low  	[4]

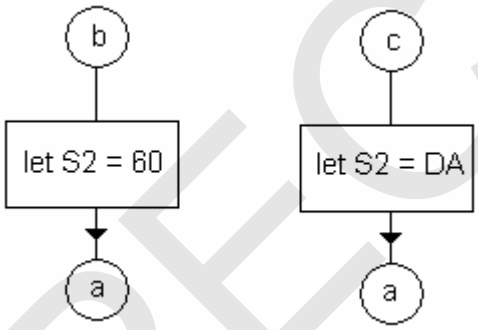
Question Number	Answer	Max Mark
3(a)	input and output correctly labelled correct circuit all resistors in range 1 kΩ to 1 MΩ feedback resistor five times input resistor justification through G = -Rf/Rin  	[5]
(b)	straight line through origin negative gain of five (by eye) saturating at ±13 V (by eye)  	[4]

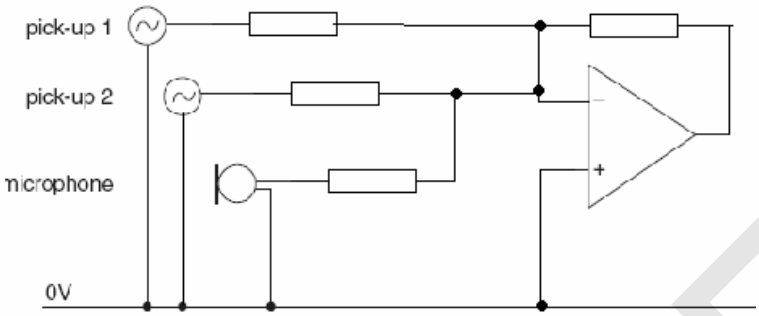
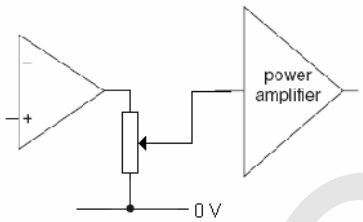
Question Number	Answer	Max Mark
4(a)	D connected to $\overline{Q}$ for each flip-flop outputs correctly labelled $\overline{Q}$ of first flip-flop to clock of second NOT gate correctly placed  	[4]
(b)	AB correct ecf: W correct ecf: Z correct ecf incorrect W/Z: L/R on when Z/R high 	[4]
(c)(i)	AND gate to reset counter reset on A.B OR gates to provide signals for L and R correct circuit for LED R (anything which works) correct circuit for LED L  	[5]

clock pulse	A	B	W	Z	L	R
0	0	0	0	0	off	off
1	1	0	1	0	off	on
2	0	1	0	1	on	off
3	1	1	0	0	off	off

Question Number	Answer	Max Mark
4(c)(ii)	counter reset when AB = 1 R on for AB = 10 and 10 L on for AB = 00 and 10 algebra of truth table to justify arrangement of logic gates This question will be assessed for quality of written communication. 3 The candidate expresses complex ideas extremely clearly and fluently. Sentences and paragraphs follow on from one another smoothly and logically. Arguments are consistently relevant and well structured. There will be few, if any, errors of grammar, punctuation and spelling. 2 The candidate expresses straightforward ideas clearly, if not always fluently. Sentences and paragraphs may not always be well connected. Arguments may sometimes stray from the point or be weakly presented. There may be some errors of grammar, punctuation and spelling, but not such as to suggest a weakness in these areas. 1 The candidate expresses simple ideas clearly, but may be imprecise and awkward in dealing with complex or subtle concepts. Arguments may be of doubtful relevance or obscurely presented. Errors in grammar, punctuation and spelling may be noticeable and intrusive, suggesting weaknesses in these areas. 0 The language has no rewardable features.	[7]
(d)	cheaper / easier same hardware but different software economies of scale / less development time / reusable	[3]

Question Number	Answer	Max Mark
5(a)	resistors for inverting amplifier circuit capacitor in parallel with feedback resistor feedback resistor 100 times input resistor resistors in range 1 kΩ to 1 MΩ $R_fC = 1.6\times10^{-4}$ s because $f_0 = 1/2\pi RC$  	[6]
(b)(i)	horizontal at 10^2 at low frequencies suddenly drops after 1 kHz at 0.1 per tenfold increase of frequency  	[3]
(ii)	idea of capacitor as resistance which drops with rising frequency why capacitor irrelevant below break frequency (in parallel ...) idea of capacitor as feedback resistor at high frequency	[3]

Question Number	Answer	Max Mark
6(a)(i)	any of the following, maximum [3] • set of registers / flip-flops which hold words • memory to store a program • input and output ports to exchange words with other systems • programmed by external computer	[3]
(ii)	hardware is the circuitry / components program is sequence of words stored in memory	[2]
(b)(i)	1111 1101	[1]
(ii)	(place FD in register S2) copy FD to output port display shows zero copy input port into register S1 jump to b: if I_7 is high i.e. only one switch pressed jump to b: if I_6 is high i.e. only the other switch pressed jump to c: if both switches are pressed no switches are pressed, so loop back to start	[7]
(iii)	Program: e.g.  word placed into S2 jump to a: / output word then stop correct bytes placed in S2 to display 1 and 2 accordingly Explanation: need to feed out 0110 0000 or 1101 1010 to get 1 or 2 displayed branching explained	[5]

Question Number	Answer	Max Mark
7(a)(i)	feedback resistor non-inverting input to 0 V resistors to inverting input from three signal inputs  	[3]
(ii)	correct symbol for potentiometer connected correctly between summing amp and power amp  	[2]
(b)(i)	use of $G = -R_f/R_{in}$ $G = (-)\ 5/100\times10^{-3} = (-)50$ ecf incorrect gain: $R_f = 50 \times 10\times10^3 = 500\ k\Omega$	[3]
(ii)	$G = 3/20\times10^{-3} = 150$ ecf incorrect R_f: $R_{in} = 500\ k / 150 = 3.3\ k\Omega$	[2]
(c)(i)	max voltage = 3 + 3 + 5 = 11 V $I = V/R$ (eor) ecf incorrect V: $I = 11/8 = \underline{1.4}$ A	[3]
(ii)	negative feedback forces both inputs to the same voltage because of high open-loop gain of op-amp	[3]
	Paper Total	**[90]**

Assessment Objectives Grid (includes QWC)

Question	AO1	AO2	AO3	Total
1(a)	1	1		**2**
1(b)	2	1		**3**
2(a)	1			**1**
2(b)		2		**2**
2(c)	2	2		**4**
3(a)	2	3		**5**
3(b)	2	2		**4**
4(a)	3	1		**4**
4(b)	2	2		**4**
4(c)(i)	2	3		**5**
4(c)(ii)	3	4		**7**
4(d)	3			**3**
5(a)	2	4		**6**
5(b)(i)	2	1		**3**
5(b)(ii)	1	2		**3**
6(a)(i)	3			**3**
6(a)(ii)	3			**3**
6(b)(i)		1		**1**
6(b)(ii)	3	4		**7**
6(b)(iii)		4		**4**
7(a)(i)	2	1		**3**
7(a)(ii)	1	1		**2**
7(b)(i)	1	2		**3**
7(b)(ii)	1	1		**2**
7(c)(i)	1	2		**3**
7(c)(ii)	1	2		**3**
Totals	**44**	**46**	**0**	**90**